

Amendments to the Claims:

1. (Currently amended) A circuit for detection of internal microprocessor watchdog device execution in a microprocessor system comprising
a microprocessor ~~with the~~ having

a reset input,

an internal watchdog device generating a reset signal and connected to the reset input,
and

an input/output line WDOG_PIO transmitting information about microprocessor reset
independently from the reset signal and;

a device for resetting the microprocessor system and having

an activation input,

a system reset output connected to the reset input of the microprocessor and
configured to generate a system reset signal at the system reset output responsively to an
activation input signal received at the activation input , wherein the input/output line (11)
transmitting information about the microprocessor (6) reset, a clock input CK is connected,
which triggers the;

a flip-flop (12), whose having

a clock input CK connected to the input/output line WDOG_PIO of the
microprocessor,

a data input D and an inverted reset input /R are connected to an the system reset
output of the device (49) for resetting the microprocessor system, and

an inverted flip-flop (42) output /Q is connected to an the activation input of the device (19) for resetting the microprocessor system.

2. (Currently amended) The circuit according to claim 1 further comprising an external resistor (40) connecting the input/output line (41) ~~transmitting information about microprocessor (6)~~ reset WDOG_PIQ to a power supply voltage (V_{cc}).
3. (Currently amended) The circuit according to claim 1, wherein reset of the microprocessor system resulting from ~~the~~ reset of the microprocessor (6) is performed when the inverted reset input /R and the flip-flop (42) data input D are in a high state and the clock input CK changes from a low to a high state.
4. (Currently amended) The circuit according to claim 1, wherein reset of the microprocessor system resulting from ~~the~~ reset of the microprocessor (6) is blocked by a low state of the inverted reset input /R of the flip-flop (42).
5. (Canceled)
6. (Canceled)
7. (Canceled)

8. (Currently amended) A circuit for detection of internal processor watchdog device execution in a microprocessor system comprising

- a microprocessor having an input/output;
- an internal watchdog device linked to the microprocessor via reset signal lines and activating the microprocessor;
- a flip-flop having
 - a data input D,
 - an inverted reset input /R connected with the data input D,
 - an inverted output /Q for resetting the microprocessor, and
 - a clock input CK connected to the input/output of the microprocessor via an input/output line transmitting information about microprocessor reset;
- a device for resetting the microprocessor and linked to the inverted output /Q and the inverted reset input /R of the flip-flop and the microprocessor; and
- an external resistor connecting the input/output line transmitting information about the microprocessor reset to a power supply voltage.

9. (New) A microprocessor system comprising:

- a microprocessor having
 - a reset input,
 - an internal watchdog device generating a reset signal and connected to the reset input of the microprocessor, and
 - an input/output line WDOG_PIO configured to transmit information about microprocessor reset independently from the reset signal;

a system reset circuit having

an activation input, and

a system reset output connected to the reset input of the microprocessor and configured to generate a system reset signal at the system reset output responsively to an activation input signal received at the activation input;

a flip-flop having

a clock input CK connected to the input/output line WDOG_PIO of the microprocessor,

a data input D and an inverted reset input /R connected to the system reset output of the system reset circuit, and

an inverted output /Q connected to the activation input of the system reset circuit.

10. (New) The microprocessor system according to claim 9, further comprising a Flash memory having a reset input connected to the system reset output of the system reset circuit.